CMOS NAND GATE BASED DOUBLE EDGE TRIGGERED FLIP-FLOP

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Abstract. This paper presents the new design of double-edge triggered flip-flop using CMOS NAND gate and CMOS NAND gate with glitch removal technique these designs compare with existing double edge triggered flip-flop using C-element. Characteristic of the presented flip-flop is reducing power consumption and give lesser delay time and it also reduces the glitch using path balancing technique. CMOS NAND gate double edge triggered flip-flop has lesser number of transistors as compared to double edge triggered flip-flop using C-element. Here simulate the double edge triggered flip-flop at 16nm technology and compare the power and time delay.
Keywords: Double-edge triggered flip-flop, C-element, CMOS NAND gate.

1. INTRODUCTION

Today's era is power consumption and double edge triggered flip-flop is basically known for power saving mode so, this flip-flop is the best option for reducing power consumption in circuits. The essential storage elements in digital circuits are flip-flops that play a major role in circuit power consumption and speed [3], [10]. Edge-triggered flip-flops are of two types: (single edge triggered flip-flop) SET-FF and (double edge triggered flip-flop) DET-FF. SET-FF is active either on rising edge or falling edge but DET-FF is edge sensitive so it is triggered on both the edges of flip-flop rising and falling because of this it is called DET-FF. It gives the same data throughput at the half clock frequency of SET-FF. For design, two transparent latches are placed in parallel in a DET-FF whereas in SET-FF it is placed in series. Half of the power in the clock distribution network can be saved using double edge clocking. It can also reduce the clock frequency. SET-FF takes many cycles to sample the data whereas DET-FF takes only a few cycles to pass the data [9].

The different way to make double edge triggered flip-flop, here discussed C-element and CMOS NAND gate based DET-FF. C-element basically uses for reducing switching activity to reduce glitch. CMOS NAND gate is used for reducing power consumption and time delay and with the help of glitch reducing technique reduce glitches from the circuit and make the circuit performance better. This paper is organized as follows: Division II discusses about circuit description of the existing circuit, the proposed method is discussed in Division II, simulation and results are shown in Division III and finally, the conclusion is discussed in Division V.
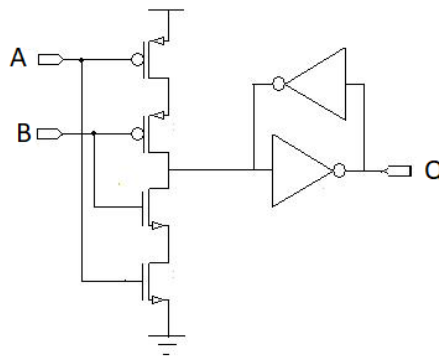
2. CIRCUIT DESCRIPTION OF EXISTING CIRCUIT

Fig.1 Transistor-level schematic diagram of C-element with weak feedback

A C-element is a two input and one output, it is a three-terminal device. The output shifts to the value of input when all of its inputs are the same. On the other hand when the inputs are not the in the same manner then the earlier output is well-preserved. It behaves like a latch which can be set or reset with the combination of signal levels at the input. In fig.1 shown

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that the two transistor level implementation of C-element with weak feedback use in this paper. The truth table of C-element is shown in table 1.

Table.1 Truth table: C-element

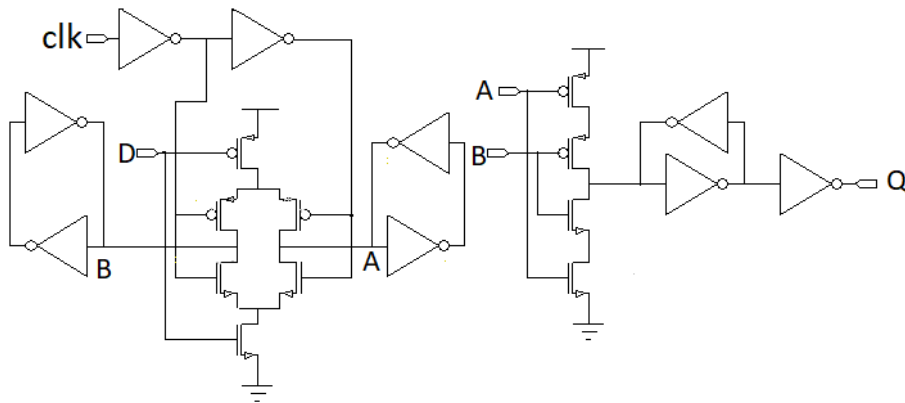| Inputs		Output
0	0	0
0	1	Cn
1	0	Cn
0	1	1

Fig.2 Schematic diagram of DET-FF based on C-element (using weak feedback in Fig.1)

In the existing design shown in Fig.2, use C-element for reducing switching activity which reduces glitches [1]. In existing design consists of two internal latches, internal nodes A and B and Q belongs to output. The latch output switches when the internal node A and B have the same signal level. At least one of A or B is latching D-bar in between clock transition. The internal node (either A or B) at D will not toggle when there is a transition in the clock signal i.e. the node which is at D-bar will toggle to have D-bar at both A and B, resulting the output C-element to switch from Q to D [2].
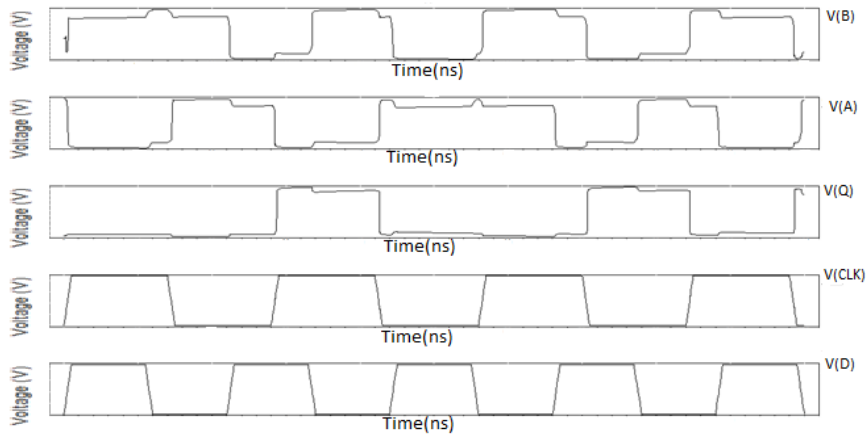Operational waveform of DET-FF based on C-element is shown in Fig.3.

Fig.3 Operational waveform of DET-FF based C-element

3. PROPOSED CIRCUIT

In proposed circuit remove the disadvantage of the existing circuit. Here make two type of proposed circuit first use CMOS NAND gate, with the help of this reduce the number of transistors. Another one is CMOS NAND gate with glitch removal technique it implemented on fewer transistors as compared to the existing circuit.

3.1 CMOS NAND gate

NAND gate is the universal gate. It is the combination of PMOS and NMOS. It has the opposite result of AND gate i.e. NAND gate is complementary of AND gate. When the inputs are high then the output of NAND gate is low. The schematic diagram of CMOS NAND gate is displayed in Fig.4.
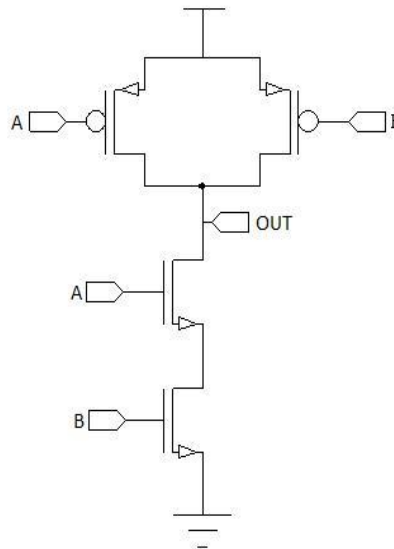

Fig.4 CMOS NAND gate

3.2 Glitch Formation and Removal

Glitch is a kind of distorted output waveform, because of crosstalk from a neighbor clocking or switching circuits or sudden turn on and off in the circuit [7]. But sometimes it is not dangerous for the circuit it depends on the circuit requirement. The signal reaches to steady state and before this state the signal might go through several state change which is glitches and they dissipate 20-70% of total power dissipation [6], because of this glitch is needed to be eliminated for low power design. Many ways to remove glitches from the circuit here use path balancing technique for glitch removal. Glitch power comes with dynamic power. It is directly proportional to switching activity. In existing design use C-element because C-element reduces switching activity [8].

When the glitch is not present in the output of any gate then the combinational circuit is minimum transient energy design. When difference at every gate inputs signal arrival time remains smaller than the inertial delay of the gate and this condition is expressed by the following equation-
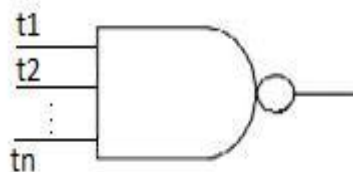
$$t_n - t_1 < d_i \tag{1}$$
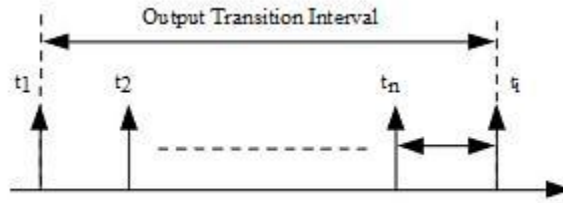
Here t_1 is the initial arrival time at inputs,

t_n is the arrival time at another input that is the most delayed,

d_i is the gate"s inertial delay.

To satisfy inequality, either increase the gates inertial delay (hazard filtering) or decrease the path difference $t_n - t_1$ (path balancing).
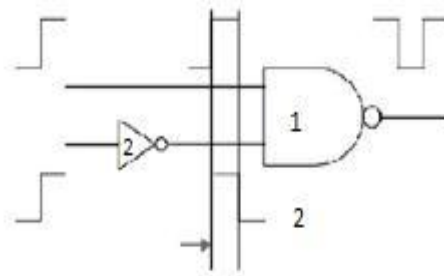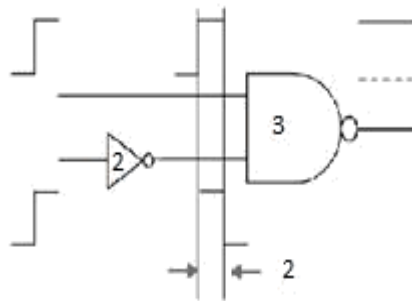

(a)

(b)
Fig.5.Symbol of n-input NAND gate and their transition time are shown in (a) and
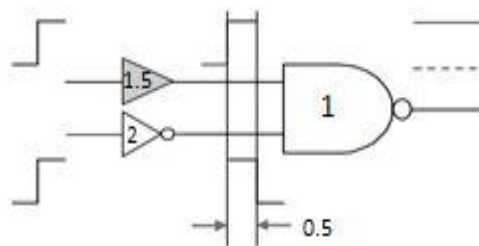
(b) respectively.

(a)   A NAND gate with glitch at the output end

(b)   Glitch elimination using hazard filtering technique

Glitch elimination by using path delay balancing Fig.6 Glitch elimination methods

3.3 Proposed circuit (I)

In proposed circuit is shown in Fig.7, CMOS NAND gate based double edge triggered flip-flop.
In proposed circuit design use CMOS NAND gate instead of C-element. It is implemented on less number of transistors. It reduces the power consumption and it has the lesser delay time. It has two internal latches A and B, these are the internal nodes and D is the input and here Q is the circuit output. The operational waveform is shown in Fig.8.
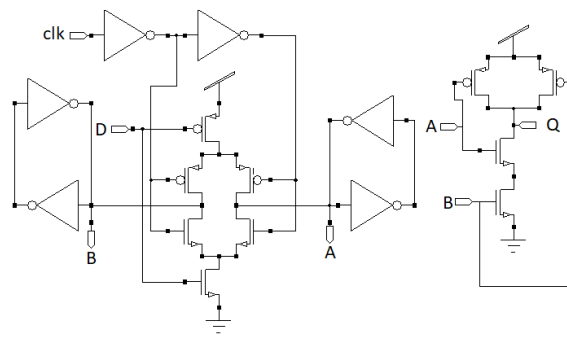
Fig.7 Schematic diagram of proposed circuit using CMOS NAND gate

The output of this circuit depends on A and B, as shown in Fig. 8 when the clock „Clk" is in "high" state and the input „D" is also "high" then the output Q is also in "high" state. When the clock is "low" while the input D is in "high" state then the output of this circuit is in "low". When the clock „Clk" is "low" and the input D is in "low" state then Q output is in "high" state. When the clock „Clk" is "high" and the input D is in "low" state then the output of this circuit is in "high" state.
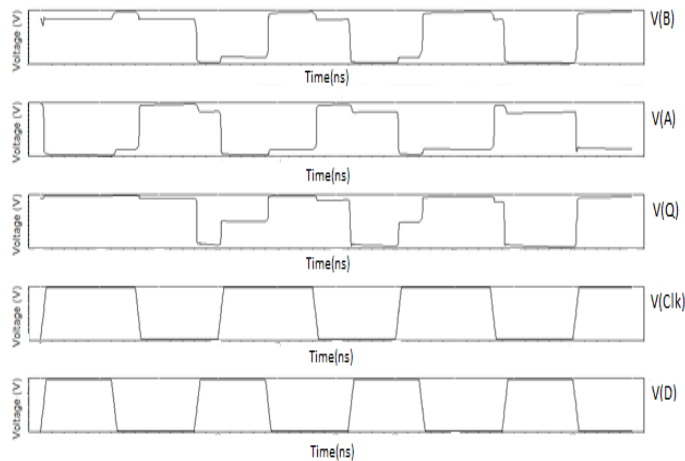

Fig.8 Output waveform of proposed circuit (I)

Power consumption is reduced approx. 30% as compared to existing circuit and delay is lesser approx. 60% as compared to the existing circuit.

3.4 Proposed circuit (II)
In proposed circuit (II) shown in Fig.9, glitch removal technique is used along with CMOS NAND gate.
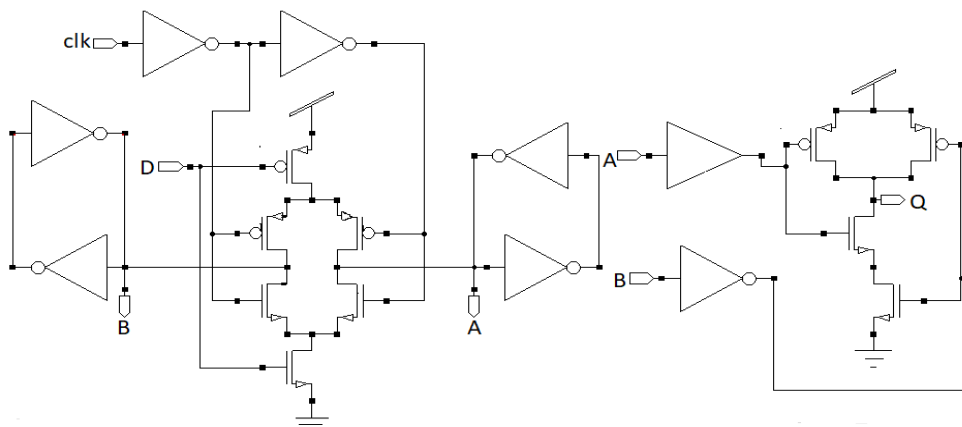

Fig.9 Schematic diagram of proposed circuit (II)

In proposed circuit (I) use CMOS NAND gate and in the proposed circuit (II) use glitch removal technique along with CMOS NAND gate. For glitch removal path balancing technique is used. It gives the glitch-free output. Operation of this design is same as the proposed circuit design (I). It reduces the power consumption by reducing glitches. The operational waveform of the proposed circuit (II) is shown in Fig. 10.
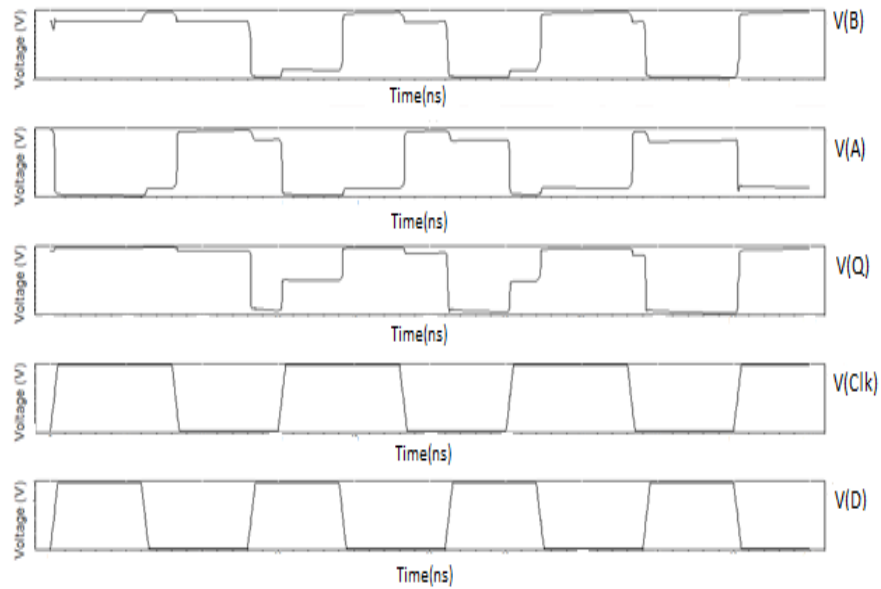

Fig. 10 output waveform of proposed circuit design (II)

It reduces approx. 50% power consumption compared to the existing circuit, the performance of the circuit is better as compared to the existing circuit.

4 SIMULATION RESULT

For circuit simulation used tanner tool (version 14.1) at 16nm technology. Check the difference between power and time delay of existing DET-FF circuit using C-element and newly proposed circuit CMOS NAND gate based DET-FF, use low voltage for the simulation. CMOS NAND gate using glitch removal techniques (proposed circuit-II) provide the better result on low voltage. Area of CMOS NAND gate based DET-FF using glitch removal technique is larger as compared to CMOS NAND gate based DET-FF circuit because transistor count is increased but it removes glitch and overall performance is good.

Table 2. Comparison among existing and proposed DET-FFs (ref.1)

Parameters	Existing circuit	Proposed circuit (I)	Proposed circuit (II)
Voltage (volt)	2.2	2.2	2.1
Average power (mw)	62.31	40.98	35.62
Rise time delay (ns)	46.18	15.18	39.23
Fall time delay (ns)	18.30	6.84	29.00
Average time delay (ns)	32.25	11.01	34.41
No. of transistors	28	22	26
Power delay product (w-ns)	2.02	0.45	1.22

5. CONCLUSION

The existing DET-FFF circuit use C-element for reducing switching activity which reduces glitch. But the disadvantage of using C-element is that it consumes more power and gives larger delay and also it implements more transistors. To overcome these problems a circuit with CMOS NAND gate has been designed.

In proposed CMOS NAND gate based DET-FF (proposed circuit-I) use CMOS NAND gate instead of C-element since it gives less power consumption and lesser power delay compared to existing double edge triggered flip-flop. It also implements less number of transistors thus covers less silicon area as compared to existing DET-FF. Therefore, the circuit design is simple and is cost effective.

The proposed CMOS NAND gate based DET-FF using glitch removal technique (proposed circuit-I) uses path balancing technique for reducing the glitch from the circuit. This technique improves the overall performance of the circuit by removing the glitch from the circuit.

As the proposed design has proven to work efficiently in terms of various performance parameters thus more effective results will be obtained when it is used in more applications like low power application and low voltage circuits like registers, memory cells etc.

6. REFERENCES

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